Claims

1. Phase/frequency-locked loop (1) having a phase/frequency comparator (8) and a frequency-generating oscillator (10), the phase/frequency comparator (8) having two edge-triggered storage devices (13, 14) which are respectively set by an edge of a reference-frequency signal (4), whose frequency may be divided if required, for the phase/frequency locked loop (1), and by an edge of an output-frequency signal (6), whose frequency may be divided if required, from the phase/frequency locked loop (1) and which are each reset by an output signal (16) from a resetting logic unit (15) to whose inputs are supplied the output signals (9A, 9B) from the two edge-triggered storage devices (13, 14), characterised in that the output signal (16) from the resetting logic unit (15) is only activated when both the output signals (9A, 9B) from the two edge-triggered storage devices (13, 14) have been activated, and is only de-activated when both the output signals (9A, 9B) from the two edge-triggered storage devices (13, 14) have been de-activated.

2. Phase/frequency-locked loop according to claim 1, characterised in that the resetting logic unit (15) is implemented by means of an asynchronous level-triggered RS storage device (17, 24).

3. Phase/frequency-locked loop according to claim 2, characterised in that the asynchronous level-triggered RS storage device (24) of the resetting logic unit (15) is set or reset by non-inverted input signals.

4. Phase/frequency-locked loop according to claim 2, characterised in that the asynchronous level-triggered RS storage device (17) of the resetting logic unit (15) is set or reset by inverted input signals.

5. Phase/frequency-locked loop according to one of claims 1 to 4, characterised in that the output (Q) of the edge-triggered storage device (13), to whose input (Clk) the reference-frequency signal (3), whose frequency may be divided if required, is applied is fed to the frequency-generating oscillator (10) to increase the frequency of the output-frequency signal (6), and the output (Q) of the edge-triggered storage device (14), to whose input (Clk) the output-frequency signal (6), whose frequency may be divided if required, is applied is fed to the frequency-generating oscillator (10) to reduce the frequency of the output-frequency signal (6).

6. Phase/frequency-locked loop according to either of claims 1 and 5, characterised in that the signals (9A, 9B) at the outputs (Q) of the two edge-triggered storage devices (13, 14) are connected to the frequency-generating oscillator (10) via an interposed loop filter (11) for stabilising the phase-frequency-locked loop (1).

7. Phase/frequency-locked loop according to one of claims 1 to 6, characterised in that the frequency of the reference-frequency signal (2) to the phase/frequency-locked loop (1) is reduced by a factor N by means of a frequency divider (2), upstream of the input (Clk) of the phase/frequency comparator (8).

8. Phase/frequency-locked loop according to one of claims 1 to 7, characterised in that the frequency of the output-frequency signal (6) from the phase/frequency-locked loop (1) is reduced by a factor M by means of a frequency divider (5), upstream of the input (Clk) of the phase/frequency comparator (8).

9. Phase/frequency comparator (8) for a phase/frequency-locked loop (1), having two edge-triggered storage devices (13, 14) which are respectively set by an edge of a reference-frequency signal (3), which may be divided if required, for the phase/frequency-locked loop (1), and by an edge of an output-frequency signal (6), which may be divided if required, from the phase/frequency-locked loop (1), and which are each reset by an output signal (16) from a resetting logic unit (15) to whose inputs are supplied the output signals (9A, 9B) from the two edge-triggered storage devices (13, 14), characterised in that the output signal (16) from the resetting logic unit (15) is only activated when both the output signals (9A, 9B) from the two edge-triggered storage devices (13, 14) have been activated, and is only de-activated when both the output signals (9A, 9B) from the two edge-triggered storage devices (13, 14) have been de-activated.

10. Phase/frequency comparator according to claim 9, characterised in that the resetting logic unit (15) is implemented by means of an asynchronous level-triggered RS storage device (17, 24).

11. Phase/frequency comparator according to claim 10, characterised in that the asynchronous level-triggered RS

storage device (24) of the resetting logic unit (15) is set or reset by non-inverted input signals.

12. Phase/frequency comparator according to claim 10, characterised in that the asynchronous level-triggered RS storage device (17) of the resetting logic unit (15) is set or reset by inverted input signals.

Captioning in Figures

Figs. 1A, 1B, 1C and 1D

Referenzfrequenz-Signal = Reference-frequency signal

Ausgangsfrequenz-Signal = Output-frequency signal

$Stell_{oben}$ = $Correct_{upward}$

$Stell_{unten}$ = $Correct_{downward}$

f_{soll} = $f_{desired}$

f_{ist} = f_{actual}

φ_{soll} = $\varphi_{desired}$

φ_{ist} = φ_{actual}

Fig. 2

Referenzfrequenz-Signal = Reference-frequency signal

(optional) = (optional)

Phasen/Frequenz-Komparator = Phase/frequency comparator

Schleifenfilter = Loop filter

Oszillator = Oscillator

Ausgangsfrequenz-Signal = Output-frequency signal

Fig. 3

Referenzfrequenz-Signal = Reference-frequency signal

Ausgangsfrequenz-Signal = Output-frequency signal

(optional) = (optional)

Rücksetzsignal = Resetting signal

$Stell_{oben}$ = $Correct_{upward}$

Rücksetzlogik = Resetting logic

$Stell_{unten}$ = $Correct_{downward}$

zum Schleifenfilter = To the loop filter

Fig. 4

$Stell_{oben}$ = $Correct_{upward}$

$Stell_{unten}$ = $Correct_{downward}$

UND = AND

ODER = OR

RS-Flip-Flop = RS flip-flop

Rücksetzsignal = Resetting signal

Fig. 5

$Stell_{oben}$ = $Correct_{upward}$

$Stell_{unten}$ = $Correct_{downward}$

UND = AND

ODER = OR

RS-Flip-Flop = RS flip-flop

Rücksetzsignal = Resetting signal